Temperature Compensated Crystal Oscillators [TCXO " M " and VCTCXO " VM "]

QuikXO™ MERCURY QUICK - TURN Oscillators

TCXO	VCTCXO	SMD	1.8 V	2.5 V	3.3 V	Min.	Max.
MJF538_	VMJF538_					15 MHz	2,100 MHz

Features

Mercury's QuikXO Quick-Turn TCXO that can be delivered in days, support high frequency up to 2.1 GHz.
mininature product size, An integrated phase jitter performance of 300 fs RMS.
Supports all popular formats: LVPECL, LVDS, HCSL and CML

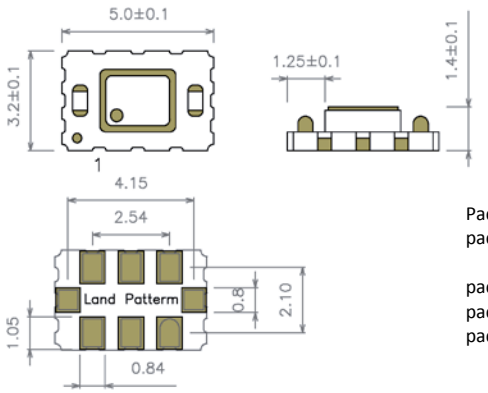
General specifications , at Ta = + 25°C

Model	(V) MJF538P	(V) MJF538D	(V) MJF538C	(V) MJF538Q
Output Logic	LVPECL	LVDS	HCSL	CML
Supply Voltage V_{DD} (code)	--	--	+ 1.8 V_{DD} ± 5%	+ 1.8 V_{DD} ± 5%
	+ 2.5 V_{DD} ± 10%	+ 2.5 V_{DD} ± 10%	+ 2.5 V_{DD} ± 10%	+ 2.5 V_{DD} ± 10%
	+ 3.3 V_{DD} ± 10%	+ 3.3 V_{DD} ± 10%	+ 3.3 V_{DD} ± 10%	+ 3.3 V_{DD} ± 10%
Available Frequency Range	15 ~ 2,100 MHz	15 ~ 2,100 MHz	15 ~ 700 MHz	15 ~ 2,100 MHz
Load	50 Ω into V_{DD} - 2V or Thevenin equivalent	100 Ω between output and complimentary output	50 Ω to GND	50 Ω to V_{DD}
Output Logic " High " , " 1 "	V_{DD} - 1.03 V min. V_{DD} - 0.6 V max.	1.4 V Typical 1.6 V max.	V_{DD} : 0.66V min. V_{DD} : 1.15V max.	V_{DD} - 0.085V min. V_{DD} = max.
Output Logic " Low " , " 0 "	V_{DD} - 1.85 V min. V_{DD} - 1.6 V max.	1.1 V Typical 0.9 V min.	V_{DD} : 0.0V min. V_{DD} : 0.15V max.	V_{DD} - 0.6V min. V_{DD} - 0.32V max.
Current Consumption (V_{DD} = + 3.3 V)	100 mA typ. 120 mA max.	75 mA typ. 90 mA max.	80 mA typ. 100 mA max.	70 mA typ. 85 mA max.
Current with Output Disabie	99 mA typical	74 mA typical	79 mA typical	69 mA typical
Rise Time / Fall Time (20% to 80% Waveform)	0.4 ns max.	0.4 ns max.	0.4 ns max.	0.4 ns max.
Initial Calibration Tolerance	± 1.0 ppm. max. at +25°C ± 2°C.			
Frequency Stability Codes	Temperature (ref to +25°C)	± 2.5 ppm over -40°C to +85°C (default)		
		± 1.5 ppm over -40°C to +85°C (available)		
	Aging	± 1.0 ppm max . , per year at 25°C		
	Voltage Change	± 0.2 ppm max . , for a ± 5% input voltage change.		
	Load Change	± 0.2 ppm max . , for a ± 10% load condition change.		
	Reflow	± 1.0 ppm max . , 1 reflow and measured 24 hours afterwards.		
Duty Cycle	50 % ± 5%		Aging at Ta = +25°C	± 3 ppm max. for first year at 25°C
Start-up Time	5 m sec (typ.) ; 10 m sec. (max.)		Storage Temperature	-55°C to + 150°C
Phase Jitter , rms (typical) (12 KHz to 20 MHz)	15 MHz ~ 50 MHz : 500 fsec typical , 51MHz ~ 1,200 MHz : 250 fsec typical			

Control Voltage Function on Pad 1		Output Enable Function on pad 2	
Control Voltage Center and Range	+1.5V ± 1.0V for both V_{DD} = 2.5V and 3.3V	Output Enable / Disable Function	70% of V_{DD} (min.) to enable output.
	+ 0.9V ± 0.6V for both V_{DD} = 1.8V		30% of V_{DD} (max.) to disable output
Frequency Pulling Range	± 8 ppm min.	Ouput Enable Time	200 ns. Max.
Linearity	± 1 % typical. ± 10% max.		
Transfer Function	Positive Transfer	Output Disable Time	50 ns. Max.
Input Impedance	5 MΩ typical.		

Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs

MJF538_ , VMJF538_



Pad Connection :
pad 1 : VCTCXO : Control Voltage
TCXO : Ground
pad 2 : OE
pad 3 : Ground
pad 4 : output
pad 5 : Complimentary output
pad 6 : Supply Voltage
pad 7 : Do Not Connet
pad 8 : Do Not Connet

A3

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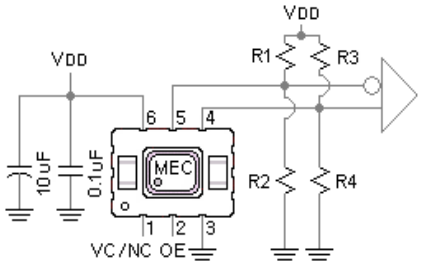
Part Number Format and Example

Example : MJF538D33-100.000-2.5/-40+85

MJF	538	D	33	-	100.000	-	2.5	/	-40+85
Hold Type	Package Size	P : LVPECL	Supply Voltage		Center Freq. (MHz)		Freq. Stability (ppm)		Operating
" **MJF** " : TCXO	" **538** "	D : LVDS	" **33** " for 3.3V						Temperature
" **VMJF** " : VCTCXO	(5.0 * 3.2 mm)	C : HCSL	" **25** " for 2.5V						Range(℃)
	8pad	Q : CML	" **18** " for 1.8V						

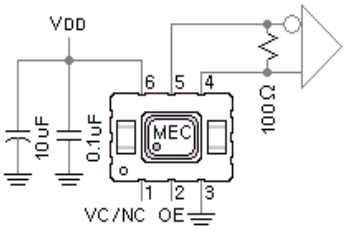
Test Circuits and Output Waveforms

LVPECL Test Circuit



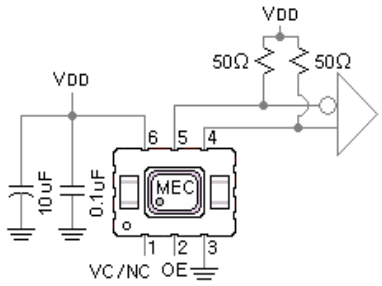
VDD = 3.3 V : R1 = R3 = 127Ω ; R2 = R4 = 82.5Ω
VDD = 2.5 V : R1 = R3 = 250Ω ; R2 = R4 = 62.5Ω

LVDS Test Circuit

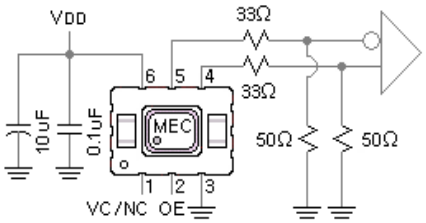


± 1.5 ppm over -40℃ to +85℃ (default)
± 1.0 ppm over -40℃ to +85℃ (available)

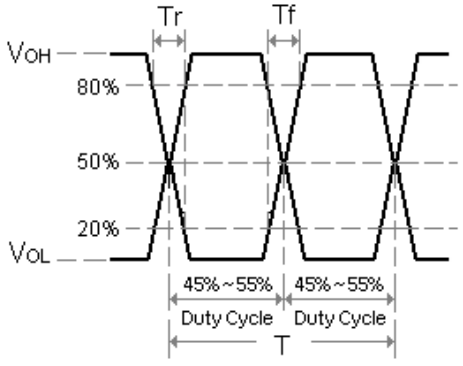
CML Test Circuit



HCSL Test Circuit



Differential Output Waveforms



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